IN THE CLAIMS

Please amend the claims as follows:

1-12. (Cancelled)

13. (Previously Presented) A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute said clock signal to multiple clocked elements within said microelectronic die using salphasic clocking techniques, said clock signal distribution network including at least one on-die interconnect section comprising first and second differential signal lines on a first metal layer of said microelectronic die to carry a differential version of said clock signal, said first and second differential signal lines being substantially parallel to one another, wherein the first and second differential signal lines each have widths such that the widths and a spacing between the first and second differential signal lines are selected to reduce inductance losses with a signal return path on a second metal layer of said microelectronic die.

14. (Previously Presented) The microelectronic die of claim 13, comprising:

at least one trace on the second metal layer of said microelectronic die, said at least one trace being capacitively coupled to and non-parallel with said first and second differential signal lines.

15. (Original) The microelectronic die of claim 14, wherein:

said at least one trace is substantially orthogonal to said first and second differential signal lines.

16. (Original) The microelectronic die of claim 13, wherein:

said clock signal is sinusoidal.

17. (Original) The microelectronic die of claim 13, wherein:

said first and second differential signal lines are part of a clock grid within said clock distribution network.

18. (Original) The microelectronic die of claim 13, wherein:

said first and second differential signal lines are part of an H-tree within said clock distribution network.

19-25. (Cancelled)

26. (Previously Presented) The microelectronic die of claim 13, wherein said microelectronic die includes microprocessor circuitry.

27. (Previously Presented) A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute the clock signal to multiple clocked elements within the microelectronic die using salphasic clocking techniques, the clock signal distribution network including a number of on-die interconnect sections having first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential version of the clock signal, the first and second differential signal lines being substantially parallel to one another; and

a number of conductive links, wherein a first conductive link of the number of conductive links couples the first differential signal line of a first one of the interconnect sections to the first differential signal line of a second one of the interconnect sections and a second conductive link of the number of the conductive links couples the second differential signal line of the first one of the interconnect sections to the second differential signal line of the second one of the interconnect sections.

28. (Previously Presented) The microelectronic die of claim 27, wherein said microelectronic die includes microprocessor circuitry.

29. (Currently Amended) ~~The microelectronic die of claim 27,~~ A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute the clock signal to multiple clocked elements within the microelectronic die using salphasic clocking techniques, the clock signal distribution network including a number of on-die interconnect sections having first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential version of the clock signal, the first and second differential signal lines being substantially parallel to one another; and

a number of conductive links, wherein a first conductive link of the number of conductive links couples the first differential signal line of a first one of the interconnect sections to the first differential signal line of a second one of the interconnect sections and a second conductive link of the number of the conductive links couples the second differential signal line of the first one of the interconnect sections to the second differential signal line of the second one of the interconnect sections, wherein the multiple clocked elements are coupled to the clock distribution network at locations where the clock signal has a signal phase independent of the position of the locations.

30. (Currently Amended) The microelectronic die of claim [[27]] 29, wherein the clock signal distribution network includes a salphasic clock gird in which the clock signal has a signal phase that is substantially position independent for the entire salphasic clock gird.

31. (Previously Presented) The microelectronic die of claim 27, further including a number of traces on a second metal layer of the microelectronic die, the number of traces being capacitively coupled to and non-parallel with the first and second differential signal lines.

32. (Previously Presented) The microelectronic die of claim 31, wherein the number of traces are substantially orthogonal to the first and second differential signal lines.

33. (Previously Presented) The microelectronic die of claim 31, wherein the number of traces includes signal lines or power lines.

34. (Previously Presented) A microelectronic die comprising:

a clock signal source to provide a clock signal; and

a clock signal distribution network to distribute the clock signal to multiple clocked elements within the microelectronic die using salphasic clocking techniques, the clock signal distribution network including an on-die interconnect section having first and second differential signal lines on a first metal layer of the microelectronic die to carry a differential version of the clock signal, the first and second differential signal lines, having a resistance per unit length, being substantially parallel to one another with a spacing between the first and second differential signal lines; and

a number of traces on a second metal layer of the microelectronic die, the number of traces being capacitively coupled to and non-parallel with the first and second differential signal lines providing a high inductance return path to the clock signal propagating on the first and second differential, the high inductance return path having an inductance per unit length, wherein a width for each of the first and second differential signal lines and the spacing between the first and second differential signal lines are selected to decrease loss by decreasing a ratio of the resistance per unit length to the inductance per unit length.

35. (Previously Presented) The microelectronic die of claim 34, wherein the number of traces are substantially orthogonal to said first and second differential signal lines.

36. (Previously Presented) The microelectronic die of claim 34, wherein the clock signal is sinusoidal.

37. (Previously Presented) The microelectronic die of claim 34, wherein the first and second differential signal lines are part of a clock grid within the clock distribution network.

38. (Previously Presented) The microelectronic die of claim 34, the first and second differential signal lines are part of an H-tree within said clock distribution network.

39. (Previously Presented) The microelectronic die of claim 34, wherein the multiple clocked elements are coupled to the clock distribution network at locations where the clock signal has a signal phase independent of the position of the locations.

40. (Previously Presented) The microelectronic die of claim 34, wherein the clock signal distribution network includes a salphasic clock gird in which the clock signal has a signal phase that is substantially position independent for the entire salphasic clock gird.

41. (Currently Amended) The microelectronic die of claim 34, further including a number of on-die interconnect sections having ~~first~~ third and ~~second~~ fourth differential signal lines and a number of conductive links, wherein a first conductive link of the number of conductive links couples the ~~first~~ third differential signal line of a first one of the interconnect sections to the ~~first~~ third differential signal line of a second one of the interconnect sections and a second conductive link of the number of the conductive links couples the ~~second~~ fourth differential signal line of the first one of the interconnect sections to the ~~second~~ fourth differential signal line of the second one of the interconnect sections.

42. (Previously Presented) The microelectronic die of claim 34, wherein the clock signal distribution network includes a salphasic clock gird having a number of locations at which the clock signal is fed to the salphasic clock gird.

43. (Previously Presented) The microelectronic die of claim 42, further including buffer units at the number of locations, the buffer units having small, differential outputs to drive the clock signal.

44. (Previously Presented) The microelectronic die of claim 42, wherein the salphasic clock gird provides the clock signal having a signal phase that is substantially position independent for the entire salphasic clock gird.

45. (Previously Presented) The microelectronic die of claim 42, wherein the clock signal distribution network includes a salphasic clock gird in which the clock signal has a signal phase that is substantially position independent for the entire salphasic clock gird.

46. (New) The microelectronic die of claim 29, further including a number of active elements coupled to a number of points in the clock signal distribution network to provide gain to the clock signal.

47. (New) The microelectronic die of claim 29, wherein the microelectronic die is a microprocessor die.